REMARKS

An excess claim fee payment letter is submitted herewith for two (2) excess claims.

Claims 1-24 are all the claims presently pending in the application. Claims 1-22 stand rejected only on informalities. There are no prior art rejections. Applicant gratefully acknowledges the Examiner's indication that claims 1-10 and 15-19 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112, second paragraph. Applicant reserves the opportunity to rewrite dependent claims 2-10 and 15-19 into independent form later. This Amendment amends claims 1, 11-14, and 20-22. Claims 23 and 24 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made to merely clarify the language of each claim, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 20 and 21 stand rejected under 35 U.S.C. §112, first paragraph.

Claims 1-22 stand rejected under 35 U.S.C. §112, second paragraph.

The rejections are respectfully traversed in view of the following discussion.

II. THE 35 U.S.C. §112, FIRST PARAGRAPH, REJECTION

Claims 20 and 21 are amended to clarify the meaning of the terms "MSB" and "LSB."

Taking the present Application as a whole, such acronyms are well known in the art and certainly would be known by any one of ordinary skill. Specifically, the claims are amended to recite "most significant bit" in place of "MSB," and the terms "least significant bit" in place of "LSB." Corresponding references to "MSB" and "LSB" in the specification have been amended to define the terms, without adding any new matter to the specification.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

Claims 1-22 were rejected for informalities. Claim 1 has been amended, specifically to cite "said detectors" to correct for the limitation's antecedent basis. Claims 11-14 have been amended to select the desired ranges of resistance for each claim.

Claim 22 has been amended to correct for informalities, as cited by the Examiner.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

The specification has been amended to correct for informalities other textual errors.

In view of the foregoing, Applicant submits that claims 1-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed

below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 6, lines 14-24 was amended, as follows:

In imaging devices composed of a plurality of pixels, there are usually variations between the pixels. These variations between the pixels may be caused by variation between detectors such as bolometers or variations in threshold voltages and parasitic capacitances of amplifying elements. In a bolometer-type infrared imaging device, for example, bolometer resistances vary from several [%] percentages to several tens [%] of percentages due to variations of the thickness of bolometer films, variations of specific resistances, and variations of patterned dimensions.

Page 10, lines 12-22 was amended, as follows:

The imaging circuit may further comprise means for comparing signals from pixels of the detectors with an upper or lower limit of a dynamic range of the reading circuit, means for generating variation data of the detectors based on the result of the comparison, and means for manipulating [an MSB] a most significant bit (MSB) of each of the variation data of the detectors to determine a value of the MSB based on the result of the comparison, and successively manipulating bits of the variation data of the detectors to determine values of the bits up to [an LSB] a least significant bit thereof.

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Page 15, line 22 to page 16, line 16 was amended, as follows:

The emitter sizes (m) of the NPN transistors 116 are different for the following reasons: The relationship between the base current I_B and the base-to-emitter voltage V_{BE} is expressed by

$$[I_B = mIB_0 Exp[qV_{BE}/k/T]] \qquad \underline{I_B = mIB_0 Exp[qV_{BE}/kT]}$$

where IB_0 represents a reverse leakage current, q a unit charge, k the Boltzmann's constant, and T the absolute temperature. Since the base current is expressed by $I_B = I_c/\beta$ where β is the current amplification factor, if the collector current changed with the emitter size m being constant, the base-to-emitter voltage V_{BE} would also change. Because the same voltage V_{b1} is applied to the bases of the transistors 116, if the base-to-emitter voltage V_{BE} were different from state to state, the currents in the respective stages would not be established as described above. By changing the emitter size m depending on the current, the base-to-emitter voltages V_{BE} in the respective stages become equal to each other, and currents in the respective stages can be established as described above.

Page 17, line 14 to page 18, line 5 was amended, as follows:

The total noise can be reduced by increasing the emitter resistance. If the emitter resistance is increased to [1 K½] 1 KΩ or more, the total noise starts to decrease. If the emitter resistance is 5 KΩ or higher, the total noise is about 3 dB lower than if the emitter resistance is 1 KΩ or less. The value of 3 dB is a limit value at which the human eye can recognize the improved total noise. When the collector current is 10 μA, then the voltage across the emitter resistance is 5 V or lower if the emitter resistance is 500 kΩ or less, and

can be handled by an ordinary BiCMOS circuit. If the emitter resistance is 100 kΩ or less, then the voltage across the emitter resistance is 1 V or less, providing a margin to the dynamic range of the circuit. Therefore, the emitter resistance should range from 1 kΩ to 500 kΩ, preferably from 5 kΩ to 100 kΩ.

Page 18, line 18 to page 19, line 10 were amended, as follows:

In order to reduce temperature drifts of the imaging device, it is necessary to reduce the temperature dependency of the currents I_0, 2 I_0, 4 I_0, . . . of the FPN correction regulated constant-current source 113. To meet this requirement, a base voltage V_{b3} serving as a basis for the currents I_0, 2 I_0, 4 I_0, . . . is designed so as to be less temperature [dependence] dependent. The base voltage V_{b3} may be generated within or supplied from outside of the FPN correction regulated constant-current source 113. For reduced temperature dependency, however, it is preferable to use a regulated constant-voltage source having a very small temperature dependency property such as a band gap reference or the like for generating the base voltage V_{b3}. In infrared imaging device applications, such a regulated constant-voltage source may be formed on a chip for a constant temperature because the chip may be or kept at a normal temperature by a Peltier device.

Page 30, lines 8-20, was amended, as follows:

Fig. 8 shows a process of generating the FPN correction data. It is assumed that the number of bits of the FPM correction data is 3. The process shown in Fig. 8 comprises a step 601 of clearing data of all addresses of the FPN memory 513, a step 602 of changing bit

positions from [MSB to LSB] most significant bit (MSB) to least significant bit (LSB), a step 603 of setting a bit b of all addresses of the FPN memory 513 to 1, an instruction step 604 for changing V addresses, an instruction step 605 of changing H addresses, a step 606 of making a conditional jump based on the decision made by the comparator 511, and a step 607 of resetting a bit b of a certain address of the FPN memory 513 to 0.

IN THE CLAIMS:

The claims were amended to read as follows:

1. (Amended) An imaging device comprising:

a plurality of detectors for converting an electromagnetic radiation into electric signals;

a plurality of read circuits, each connected to at least one of said [detector] detectors, and including a first regulated constant-current source for supplying a constant bias current to said detectors, and a second regulated constant-current source connected to said first regulated constant-current source, for correcting variations inherent in said detectors.

11. (Amended) An imaging device according to claim 5, wherein said resistance ranges from approximately 1 kΩ to 500 kΩ [, and preferably from 5 kΩ to 100 kΩ].

12. (Amended) An imaging device according to claim 6, wherein said resistance ranges from approximately 1 kΩ to 500 kΩ [, and preferably from 5 kΩ to 100 kΩ].

13. (Amended) An imaging device according to claim 9, wherein said resistance ranges from <u>approximately</u> 1 kΩ to 500 kΩ [, and preferably from 5 kΩ to 100 kΩ].

14. (Amended) An imaging device according to claim 10, wherein said resistance ranges from <u>approximately</u> 1 kΩ to 500 kΩ [, and preferably from 5 kΩ½ to 100 kΩ].

20. (Amended) An imaging device according to claim 16, further comprising means for manipulating [an MSB] <u>a most significant bit</u> of each of the variation data inherent in said detectors to determine a value of the [MSB] <u>most significant bit</u> based on the result of the comparison, and successively manipulating bits of the variation data of said detectors to determine values of the bits up to [an LSB] <u>a least significant bit</u> thereof.

21. (Amended) An imaging device according to claim 17, further comprising means for manipulating [an MSB] <u>a most significant bit</u> of each of the variation data inherent in said detectors to determine a value of the [MSB] <u>most significant bit</u> based on the result of the comparison, and successively manipulating bits of the variation data of said detectors to determine values of the bits up to [an LSB] <u>a least significant bit</u> thereof.

22. (Amended) An imaging device comprising:

a plurality of detectors arranged in a two-dimensional matrix, for converting electromagnetic radiation into electric signals;

a plurality [for] <u>of</u> switching means, each associated with said [detector for selecting

the associated detector] detectors, wherein each of said switching means selects at least one of said detectors;

a plurality of read-out circuits, each connected to said detectors in [each] a column direction;

a plurality of regulated constant-current [source] sources, each connected to [said] one of the read-out [circuit] circuits, for correcting variations inherent in said detectors;

a plurality of data buffers, each connected to said regulated constant-current [source] sources, for storing [date] data for fixed-pattern-noise correction to be supplied to said regulated constant-current [source] sources;

a plurality of multiplexers, each associated with said read-out [circuit] circuits, for selecting and outputting the output from the [associated read circuit] read-out circuits;

a vertical shift register for outputting vertical selection signals to successively turn on said switching means in [the] a plurality of respective rows of the matrix; and

a horizontal shift register for outputting horizontal selection signals to successively select said multiplexers.